# P P SAVANI UNIVERSITY

**Forth Semester of B. Tech. Examination**

**December 2022**

**SECE2040 Computer Organization**

**01.12.2022, Thursday** **Time: 01:00 p.m. To 03:30 p.m.** **Maximum Marks: 60**

***Instructions:***

1. The question paper comprises of two sections.
2. Section I and II must be attempted in separate answer sheets.
3. Make suitable assumptions and draw neat figures wherever required.
4. Use of scientific calculator is allowed.

## SECTION – I

| | | | | |
|---|---|---|---|---|
| **Q - 1** | Answer the Following (Any Five) | **[05]** | **CO** | **BTL** |
| **(i)** | _____unit of CPU co-ordinates various operations using timing signals. | | **2** | **1** |
| **(ii)** | What is concerned with the way the hardware components operate to form computer system?<br>a. Computer organization b. Computer design.<br>c. Computer architecture d. Computer implementation. | | **3** | **3** |
| **(iii)** | What is Assembler? | | **2** | **2** |
| **(iv)** | What is the use of PC (Program Counter) register in basic computer? | | **3** | **4** |
| **(v)** | Perform Arithmetic Shift left on following binary number(100110011)2 | | **4** | **5** |
| **(vi)** | Define : Control word | | **3** | **4** |
| **(vii)** | HLT is _____ type of instruction. | | **1** | **1** |
| **Q - 2 (a)** | Convert the following numbers to the bases indicated.<br>a. $(7562)_{10}$ to binary<br>b. $(1938)_{8}$ to hexadecimal<br>c. $(1001.1010)_{2}$ to decimal<br>d. $(3A)_{16}$ to decimal<br>e. $(20)_{10}$ to binary | **[05]** | **2** | **1** |
| **Q - 2 (b)** | Explain memory reference and register reference instruction code format with example. | **[05]** | **3** | **5** |
| | **OR** | | | |
| **Q - 2 (a)** | Explain Stored Program Organization with one processor register and an instruction code format with two parts. | **[05]** | **2** | **1** |
| **Q - 2 (b)** | Draw the First pass of an Assembler | **[05]** | **3** | **5** |
| **Q - 3 (a)** | Show the contents of register E, A, Q and SC during the process of multiplication of two binary numbers, 11111(multiplicand) and 10101(multiplier).The signs are not included. | **[05]** | **1** | **2** |
| **Q - 3 (b)** | Design a Flowchart for addition and subtraction of two binary numbers A and B. Assume that the numbers are stored in signed-magnitude representation. | **[05]** | **2** | **3** |
| | **OR** | | | |
| **Q - 3 (a)** | Write an assembly language program to subtract two numbers. | **[05]** | **1** | **2** |
| **Q - 3 (b)** | Show the contents of register E, A, Q and SC during the process of division of 10010011 by 1011. (Use a dividend of eight bits). | **[05]** | **2** | **3** |
| **Q - 4** | List out the tables used during second pass of assembler. Draw flowchart to explain second pass of assembler. | **[05]** | **3** | **5** |

## SECTION – II

| | | | | |
|---|---|---|---|---|
| Q - 1 | Answer the Following (Any Five) | [05] | | |
| (i) | What is bubble inside pipeline? | | 1 | 2 |
| (ii) | Define: Associative Memory | | 4 | 3 |
| (iii) | What is Peripheral Device? | | 3 | 4 |
| (iv) | Define : Logical address | | 4 | 4 |
| (v) | Determine the number of clock cycles that processor takes to process 200 tasks in a six- segment pipeline. | | 2 | 1 |
| (vi) | _____ is used to manage the transfer directly between the IO device and memory. | | 3 | 2 |
| (vii) | Define: Interface | | 1 | 3 |
| Q - 2 (a) | Explain with example: Associative mapping, Direct mapping, and Set-Associative mapping. | [05] | 1 | 2 |
| Q - 2 (b) | What is parallel processing? How Flynn's classification divides computers into four major components? | [05] | 2 | 3 |
| | **OR** | | | |
| Q - 2 (a) | Explain the different types of memory used in Computer Organization. | [05] | 1 | 2 |
| Q - 2 (b) | Explain pipelining technique. Draw the general structure of four segment pipeline. | [05] | 2 | 3 |
| Q - 3 (a) | Differentiate between source initiated and destination initiated strobe method for data transfer. | [05] | 3 | 1 |
| Q - 3 (b) | Differentiate between CISC and RISC. | [05] | 4 | 4 |
| | **OR** | | | |
| Q - 3 (a) | Differentiate between memory mapped I/O and isolated I/O? | [05] | 3 | 1 |
| Q - 3 (b) | What is DMA? With the supporting diagram, explain the functionality of DMA controller with the use of all registers and control logics. | [05] | 4 | 4 |
| Q - 4 | What is cache memory? Explain the organization of cache using Direct mapping. | [05] | 2 | 5 |

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CO : Course Outcome Number BTL : Blooms Taxonomy Level

Level of Bloom's Revised Taxonomy in Assessment

| | | |
|---|---|---|
| 1: Remember | 2: Understand | 3: Apply |
| 4: Analyze | 5: Evaluate | 6: Create |